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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/944,230	08/30/2001	John Whitman	4294.1US (98-1208.1)	2488
24247	7590 11/03/2004		EXAMINER	
TRASK BRI		DICKE		HOMAS L
P.O. BOX 2550			ART UNIT	PAPER NUMBER
SALTLAKE	CITY, UT 84110		ARTONII	TATER NOMBER
			2826	

DATE MAILED: 11/03/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

	Application No.	Applicant(s)	
	09/944,230	WHITMAN ET AL.	
Office Action Summary	Examiner	Art Unit	
·	Thomas L Dickey	2826	LANG.
The MAILING DATE of this communication app Period for Reply	ears on the cover sheet with the c	orrespondence ad	ldress
A SHORTENED STATUTORY PERIOD FOR REPLY THE MAILING DATE OF THIS COMMUNICATION. - Extensions of time may be available under the provisions of 37 CFR 1.13 after SIX (6) MONTHS from the mailing date of this communication. - If the period for reply specified above is less than thirty (30) days, a reply - If NO period for reply is specified above, the maximum statutory period w - Failure to reply within the set or extended period for reply will, by statute, - Any reply received by the Office later than three months after the mailing earned patent term adjustment. See 37 CFR 1.704(b). Status	86(a). In no event, however, may a reply be time within the statutory minimum of thirty (30) days will apply and will expire SIX (6) MONTHS from cause the application to become ABANDONE	nely filed s will be considered timel the mailing date of this c D (35 U.S.C. § 133).	
1)⊠ Responsive to communication(s) filed on <u>21 S</u>	Sentember 2004		
	s action is non-final.		
3) Since this application is in condition for allowa		osecution as to th	e merits is
closed in accordance with the practice under labels of Claims			io monto to
4) Claim(s) 1-24 is/are pending in the application	•		
4a) Of the above claim(s) 2 and 5-10 is/are with	drawn from consideration.		
5) Claim(s) is/are allowed.			
6) Claim(s) <u>1,3,4,11-13 and 15-24</u> is/are rejected.			
7) Claim(s) <u>14</u> is/are objected to.			
8) Claim(s) are subject to restriction and/or	election requirement.		
Application Papers			
9) The specification is objected to by the Examiner		_	
10)⊠ The drawing(s) filed on <u>24 January 2002 and 03</u>	<u>R November 2003</u> is/are: a)⊠ acc	epted or b)☐ objed	cted to by the
Examiner.			
Applicant may not request that any objection to the		` ,	
11) The proposed drawing correction filed on		ved by the Examin	er.
If approved, corrected drawings are required in rep 12) The oath or declaration is objected to by the Exa			
Priority under 35 U.S.C. §§ 119 and 120	2111111 6 1.		
<u> </u>	majority condox 25 LLC C C 440/a) (d) == (f)	
13) Acknowledgment is made of a claim for foreign a) All b) Some * c) None of:	priority under 35 U.S.C. § 119(a))-(a) or (t).	•
1.☐ Certified copies of the priority documents	s have been received		
2. Certified copies of the priority documents		on No	
3. Copies of the certified copies of the prior			Storo
application from the International Bur * See the attached detailed Office action for a list of	eau (PCT Rule 17.2(a)).		Stage
14) Acknowledgment is made of a claim for domestic	priority under 35 U.S.C. § 119(e	e) (to a provisional	application).
a) ☐ The translation of the foreign language pro- 15)☑ Acknowledgment is made of a claim for domestic			

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DETAILED ACTION

1. The response filed 09/21/2004 has been received.

Information Disclosure Statement

2. The Information Disclosure Statement filed on November 3, 2003 has been considered.

Claim Rejections - 35 USC § 102

3. The appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action have been quoted for the applicant in the action mailed 06/16/2004.

A. Claims 23,24, and 15-20 stand rejected under 35 U.S.C. 102(e) as being anticipated by YATES et al. (6,358,793).

Yates et al. discloses a semiconductor device structure with a substantially planar surface, comprising a substrate 5-10-15 including at least one recess (no #; it is the recess that is partially filled by part 90) formed therein, and a material layer 90 disposed at least partially over the substrate 5-10-15 and at least one intermediate layer 20, comprising at least one of a mask material, an insulative material, and a conductive material, namely, conductive HSG silicon, between the substrate 5-10-15 and the material layer 90, so that the material layer 90 and the at least one intermediate layer 20 each at

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least partially fill the at least one recess, wherein the surface of the material layer 90 is a substantially planar surface, is free of abrasive planarization-induced defects, and is substantially free of hills and valleys; and where at least one region of the at least one intermediate layer 20 and at least one region of the substrate 5-10-15 is exposed through the material layer 90, and the material layer 90 has a thickness that is less than a depth of the at least one recess. Note figures 11, 12, 7, and column 10 lines 1-31of Yates et al.

B. Claims 21,22,1,3, and 11-13 stand rejected under 35 U.S.C. 102(e) as being anticipated by KIKUCHI ET AL. (6,278,153).

Kikuchi et al. discloses a semiconductor device structure with a substrate 21-22-23-24-25-26 including at least one recess 23A formed therein, and a material layer 20 disposed over the substrate 21-22-23-24-25-26 and substantially filling the at least one recess 23A, wherein the surface of the material layer 20 is a substantially planar surface, is free of abrasive planarization-induced defects, and is substantially free of hills and valleys; and wherein the substrate 21-22-23-24-25-26 comprises a stacked capacitor structure 22-23-24-25-26 and the at least one recess 23A comprises at least one container 27 recessed in an insulator layer 23 of the stacked capacitor structure 22-23-24-25-26. Note figures 6B, 6F and column 19 lines 35-67 and column 20 lines 13-27 of Kikuchi et al.

With special regard to claims 3,12, and 13, Kikuchi et al. discloses that the material layer 20 comprises a mask material (note column 20 lines 14-17), the mask material

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substantially filling the at least one container 27, wherein the mask material has a thickness of (note the thickness disclosed by figure 6F) less than a depth of the at least one container 27.

C. Claims 21,22,1,23,24,15, and 16 stand rejected under 35 U.S.C. 102(e) as being anticipated by WANG (6,461,932), cited by the applicant on 11/03/03.

Wang discloses a semiconductor device structure with a substantially planar surface, comprising a substrate 40 including at least one recess 54 formed therein; and a material layer 56A disposed over said substrate 40 and substantially filling said at least one recess 54, so as to at least partially fill said at least one recess 54, wherein at least one region of said substrate 40 is exposed through said material layer 56A, and wherein the surface of said material layer 56A is a substantially planar surface, is free of abrasive planarization-induced defects, and is substantially free of hills and valleys. Note figure 4F and column 6 lines 23-51 and column 8 lines 26-39 of Wang.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 4 stands rejected under 35 U.S.C. 103(a) as being unpatentable over KIKU-CHI et al. (6,278,153) in view of DENNISON et al. (5,663,090).

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Kikuchi et al. discloses a semiconductor device structure with all the limitations of claim 4 except that the substrate include at least one conductively doped region continuous with a surface of the semiconductor substrate and adjacent the at least one recess. Note figure 6F of Kikuchi et al.

However, Dennison et al. discloses a semiconductor device structure with substrate 40 including at least one conductively doped region 41 that is adjacent to a recess (the recess being filled with lower electrode 43 of a stacked capacitor structure. Note figure 4b of Dennison et al. Therefore, it would have been obvious to a person having skill in the art to replace the substrate of Kikuchi et al.'s semiconductor device structure with the substrate including at least one conductively doped region that is adjacent a recess containing a stacked capacitor structure, such as taught by Dennison et al. in order to utilize the semiconductor device structure of Kikuchi et al. alongside a MOSFET such as taught by Dennison et al. to thus utilize the semiconductor device structure of Kikuchi et al. as the capacitor of a DRAM memory.

Allowable Subject Matter

4. Claim 14 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

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Response to Arguments

1. Applicant's arguments filed 09/21/2004 have been fully considered but they are not

persuasive.

It is argued, at page 5 of the remarks, that "Yates does not expressly or inherently

describe that the surfaces of any of the photoresist layers (e.g., layers 45, 70, and 75

shown in Figs. 17, 11, and 12, respectively) thereof have surfaces which are substan-

tially planar or substantially free of miniscule non-planar features, such as hills and val-

leys." However, it is noted that the features upon which applicant relies (i.e., surfaces

which are substantially free of miniscule non-planar features, or, except with regard to

claims 22 and 24, substantially planar) are not recited in the rejected claim(s). Although

the claims are interpreted in light of the specification, limitations from the specification

are not read into the claims. See In re Van Geuns, 988 F.2d 1181, 26 USPQ2d 1057

(Fed. Cir. 1993).

It is further argued at page 5, that "Claim 20 is further allowable since Yates neither

expressly nor inherently describes a material layer i.e, either the photoresist layer or the

resulting mask layer thereon that has a thickness which is less than the depths of the

containers thereof. The relative dimensions shown in the drawings of Yates cannot be

relied upon since Yates does not disclose that the drawings are to scale and is silent as

to dimensions." However, applicant's claim 20 is not "to scale," nor does it rely on spe-

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cific dimensions. The claim merely requires that one thing be thicker than another. Are we not to trust our eyes to compare the one to the other?

It is further argued at page 5, that "Claim 24 is additionally allowable since Yates lacks any express or inherent description that the surface of photoresist layer is substantially planar." However, the examiner takes the position that the surface disclosed by Yates, while perhaps lacking in perfect planarity, are nonetheless <u>substantially</u> planar. Why is applicant so insistent in pointing alleged deficiencies in the prior art when he has not yet described the advantages of his own invention?

It is argued at page 6 of the remarks that "The specification of Kikuchi does not expressly or inherently describe that a surface of the resist 20 is substantially planar or substantially free of miniscule nonplanar features, such as hills and valleys." However, it is noted that the features upon which applicant relies (i.e., surfaces which are substantially free of miniscule non-planar features, or, except with regard to claims 22 and 24, substantially planar) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

It is argued, at page 7 of the remarks, that "Claim 13 is additionally allowable since Kikuchi neither expressly nor inherently describes a material layer (i.e., either the resist layer or the resulting mask layer thereof that has a thickness which is less than the depths of the via-holes 23a thereof." However, it is noted that the features upon which applicant relies (i.e., a combination of via holes and a material layer wherein the thick-

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ness of the material layer is less than the depth of the via holes) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

It is argued, at page 8 of the remarks, that "Again, independent claims 1 and 15 require a material layer with a surface that is "substantially free of hills and valleys." As Wang teaches that the upper smoothening surface 62of the smoothening layer 60 thereof may include slight depressions" (i.e., valleys), Wang does not anticipate this element of either independent claim 1 or independent claim 15." However, the examiner takes the position that applicant's limitation, common to claims 1 and 15, of a material layer disposed over a substrate and substantially filling at least one recess, having a surface substantially free of hills and valleys, is met by Wang, first of all because Wang, although having a slight depression, has nothing that may be described as a "hill," and thus is free of the combination of "hills and valleys;" secondly because the slight depressions found in Wang nonetheless leave Wang substantially free of hills and valleys.

Conclusion

2. THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within

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TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thomas L Dickey whose telephone number is 571-272-1913. The examiner can normally be reached on Monday-Thursday 8-6.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J Flynn can be reached on 571-272-1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TLD 10/04

> Minhloan Tran Primary Examiner Art Unit 2826

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